REMARKS

Claims 1, 2, and 7 have been amended herein. Claims 3, 5, and 9 have been canceled herein. Such cancellation is without prejudice to further prosecution of these claims in one or more continuing applications. Claims 1, 2, 4, 6-8, and 10 remain in the application.

The subject matter of Claim 5, now canceled, has been incorporated into Claim 1. Claim 1 has also been amended to remove the phrases "first part" and "second part" and insert in their place "a measurement and display unit" and a "connection unit," respectively. These two phrases appear verbatim in Claim 2 as originally filed. See also Fig. 1 as filed and the description at page 13, lines 1-6 of the specification. Similarly, Claim 1 has been amended to recite that the measurement and display unit is "interconnected to" the connection unit. The word "interconnected" appears verbatim in Claim 2 as originally.

Claim 2 has been amended so that it tracks the amended language of Claim 1.

Claim 7 has been amended solely to correct a previously undetected typographical error.

No new matter is added. Favorable reconsideration is respectfully requested.

The following comments address the issues presented in the Office Action dated July 23, 2005 in order of their appearance in the Office Action.

Objections to Figures and Claims:

Please delete Figs. 7 and 8 as submitted by prior counsel. The application should include only Figs. 1 through 6 as originally filed.

The objections to the claims based on clarity grounds are believed to have been addressed by appropriate amendment to Claims 1 and 2. Specifically, Claim 1 has been amended to recite that the connection unit and the measurement and display unit are "interconnected." Claim 2 has been amended in a parallel fashion to recite that the connection unit and the measurement and display unit are interconnected via a cable assembly and weather proof connectors.

Rejection of Claims 1-10 Under 35 USC §112, First Paragraph:

This rejection is believed to have been overcome, in part, by appropriate amendment to the claims, as noted in the immediately previous section of this response. The remainder of this rejection is respectfully traversed.

Figs. 2, 3, and 6 are block diagrams showing the operation of the various sub-assemblies of the claimed device. As noted at page 13 of the application as filed, Fig. 2 is block diagram illustrating the measuring circuitry of the claimed invention. The line quality data detected in the circuitry shown schematically is output at 16 to the "display."

Fig. 5 shows an illustrative means of displaying the line quality data generated by the circuitry shown in Fig. 2. A three-phase system is illustrated. The data for each phase is "displayed" at 16 in Fig. 2. Fig. 5 therefore is simply a more detailed rendering of how that data is actually presented: a separate "normal," "spike/surge," and "sag" display for each of the three phases.

Fig. 3 is a more detailed block diagram of how the device analyzes whether line anomalies exist, and how those anomalies are displayed and memorized. For example, Fig. 3 shows the three voltage displays 29, 30, and 31 (one for each phase in a three-phase set up). These same displays are also presented at the top of Fig. 5. The same applies for the loss displays 32, 24, and 36 shown in Fig. 3, which are duplicated in Fig. 5. In effect, Fig. 5 shows how the display actually appears to a user (in a schematic sense), while Figs. 2 and 3 present the underlying circuitry and logic to produce the data that is ultimately conveyed to the user of the claimed invention.

Fig. 4 is a schematic of the machine settings, e.g., a delta or "Y" switch (39 and SW2), power input terminals (40, 41, 42, 43), etc. In effect, Fig. 4 is simply a schematic representation of the operating panel of the device. The central switch 46 is for selecting the type of line input (e.g., single channel, two channels, three channels, phase-to-phase, etc.).

Button 51 in Fig. 5 is activates the "learn" mode so that the device can store previously detected anomalies in memory. The underlying circuit for the "learn" mode 51 is shown in Fig. 6. Note that reference numeral 51 also appears in the upper, left-hand corner of Fig. 6. The sub-circuit, illustrated schematically, includes memory modules, as well as a comparator

48 that can output comparison date to the loss display unit for each channel being analyzed. See the output arrow to the immediate right of reference numeral 48 in Fig. 6. This output stream as illustrated in Fig. 6 is depicted in the unnumbered, three-headed arrow that descends vertically in Fig. 3 and enters the loss displays 32, 34, and 36. That is, in Fig. 3, between the top-most entries for "clock 1" and "clock 2" there are two vertically-oriented arrows. The output stream from Fig. 6 is the left-hand arrow as shown in Fig. 3, and terminates in the loss displays 32, 34, and 36.

Applicants therefore respectfully submit that the rejection of Claims 1-10 under 35 USC §112, first paragraph has been overcome. Withdrawal of the rejection is respectfully requested.

Rejection of Claims 1-4 Under 35 USC §102(e) Over Dorrough et al.:

This rejection has been rendered moot by incorporating the subject matter of Claim 5 into Claim 1. Claim 5 was not made subject to this rejection. Thus, by incorporating the subject matter of Claim 5 into Claim 1, this rejection has been obviated. Withdrawal of the rejection is respectfully requested.

CONCLUSION

Applicants submit that the application is now in condition for allowance. Early notification of such action is earnestly solicited.

Respectfully submitted,

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